



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/501,977	02/11/2000	Yoshitaka Takahashi	500.38174X00	4612

20457 7590 01/18/2002

ANTONELLI TERRY STOUT AND KRAUS
SUITE 1800
1300 NORTH SEVENTEENTH STREET
ARLINGTON, VA 22209

EXAMINER

WHITMORE, STACY

ART UNIT	PAPER NUMBER
----------	--------------

2812

DATE MAILED: 01/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/501,977

Applicant(s)

TAKAHASHI ET AL.

Examiner

Stacy A Whitmore

Art Unit

2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 February 2000.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4. 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 12-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Barrientos (5,910,899).

As for claims 12 and 13, Barrientos taught the invention as claimed, including a floorplan modification method, comprising the steps of:

[12] modifying a floorplan which is beforehand generated according to information for modifying a floorplan regarding allocation of blocks constituting a semiconductor IC; and evaluating the modified floorplan according to evaluation indices; and determining a floorplan according to an evaluation value; and [13] a LSIC produced according to a modified floorplan, wherein the modified plan is obtained by

modifying a floorplan which is predetermined according to information for modifying a floorplan regarding allocation of blocks constituting an IC, according to predetermined evaluation indices [abstract, fig. 5, col. 3, line 36 – col. 5, line 44, col. 8, line 35 – col. 9, line 38; col. 18, lines 55-67] .

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barrientos (5,910,899) in view of Ramachandran (6,002,857).

As for claim 1, Barrientos taught the invention as substantially claimed, including an information processing apparatus, comprising:

a display; a storage for storing a floorplan regarding allocation of blocks constituting a semiconductor IC, and evaluation indices for evaluating modification of the floorplan; an input device for inputting specifications for modifying the floorplan; a

processing device for modifying the floorplan according to the specification to generate a floorplan, and [abstract, fig. 5, col. 3, line 36 – col. 5, line 44, col. 18, lines 55-67].

Barrientos did not specifically teach generating a plurality of floorplans, and selecting one of the floorplans according to the evaluation indices. However, Ramachandran taught the generation of a plurality of floorplans and selection of one of the plurality of floorplans based on evaluation indices [abstract]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Barrientos and Ramachandran because adding the generation and selection of one of a plurality of floorplans based on evaluation indices would improve Barrientos' system by improving the speed with which the floorplans can be evaluated [see Ramachandran, abstract] which would improve the overall design time of Barrientos' system of circuit design.

As for claim 2, Barrientos taught circuit information in which the blocks are described in a high-level language is stored in the storage [see as cited in the rejection of claim 1, especially col. 5].

As for claim 3, Barrientos taught the evaluation indices include know-how of a designer who designs the semiconductor IC [see as cited in the rejection of claim 1, especially col.'s 3-4 and 18].

As for claim 4, Barrientos further taught the processing device stores a function of each of blocks constituting the semiconductor IC, a floorplan which is allocation information of the blocks, and evaluation indices used when the floorplan is modified, in the storage

Art Unit: 2812

with being associated with each other, the function, the floorplan, and the evaluation indices being inputted from the input device [see also the cited portions of the rejection of claim 1].

Claims 5-9 have similar limitations as rejected claims 1-4, and are rejected for the same reasons as cited in the rejection of claims 1-4.

As for claim 10, Barrientos further taught a program [col. 8, line 40].

Claim 11 is rejected for the same reasons as cited in the rejections of claims 1, 3, and 10.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6,170,080 Ginetti

4,918,614 Modarres

EP 0294188 A2 Modarres

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A Whitmore whose telephone number is (703) 305-0565. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers for

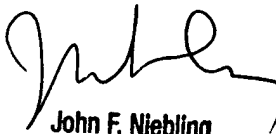
Application/Control Number: 09/501,977
Art Unit: 2812

Page 6

the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Stacy Whitmore
January 15, 2002


John F. Niebling
Supervisory Patent Examiner
Technology Center 2800